Reg No.:_____ Name:_____

00000EC207121901

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Third Semester B.Tech Degree (S,FE) Examination January 2022 (2015 Scheme)

Course Code: EC207

Course Name: LOGIC CIRCUIT DESIGN (EC, AE)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks. Marks

1 a) Convert the octal numbers 413.52 and 576.43 into binary, hexadecimal and decimal. (6)

b) Given the binary numbers a=1010.1, b=101.01 and c=1001.1 (4)
Perform the binary operations (i) a + c (ii) a – b

c) Hamming code was used to generate parity for a nibble. If received bit sequence is 1011001, check whether any error is occurred with even parity. Find the correct bit sequence if there is any error. (5)

2 a) Reduce the following functions using K-map (8)

$$f(A,B,C,D) = \sum m(0,1,3,7,15) + \sum d(2,11,12)$$

b) Implement the following function using an 8 X 1 MUX. (7)

$F(A,B,C,D) = \Sigma m\ (1,2,3,7,9,10,12,14,15)$

3 a) Design BCD to 7 segment decoder and implement it. (12)

b) Perform the conversions: (3)

i) $(10011010110101)_{BCD}$ to Decimal

ii) $(159)_{10}$ to Excess-3 code

iii) $(1010110101011)_2$ to Gray code

PART B

Answer any two full questions, each carries 15 marks.

4 a) Compare PROM, PLA and PAL. (4)

b) Draw the circuit and explain the operation of two input TTL NAND gate using totem pole. (5)

c) Implement 3 bit binary to Excess-3 converter using PLA. (6)

5 a) Convert a T flip flop to J K Flip flop (6)

b) Design a synchronous self starting counter to count the sequence 0,1,3,4,5,7,0,1... … using T flip flops. When the counter enters an unused state, the counter has to start counting from 0. (9)

6 a) Implement the following Boolean functions using PLA. (6)

$f1(A,B,C) = \sum m(0,1,3,5)$ $f2(A,B,C)=\sum m(0,2,5,7,9,10,12,14,15)$

b) Design a mod-12 synchronous counter using T flip-flop. (9)

PART C

Answer any two full questions, each carries 20 marks.

7 a) Draw the logic diagram of a four bit, bi-directional serial in serial out (SISO) shift register with LOAD/SHIFT control and explain the working with timing diagram. (8)

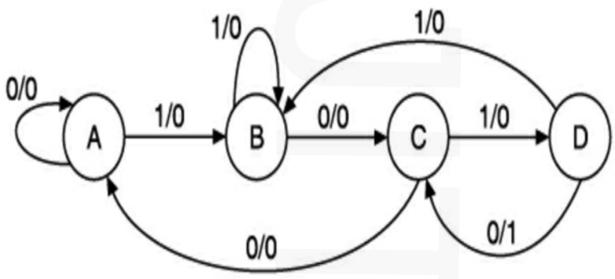
b) Differentiate Moore and Mealy models with example state diagram. (6)

c) Draw the logic diagram of a 3 bit Johnson counter and explain the working with truth table. (6)

8 a) Reduce the given state table using partition method and obtain the equivalent states. (10)

Present state	Next State		Output	
	X=0	X=1	X=0	X=1
A	C	B	1	0
B	D	C	0	0
C	G	D	0	0
D	E	F	1	0
E	A	F	1	0
F	G	F	1	0
G	A	D	0	0

b) Design a circuit to implement the given state diagram. (10)



9 a) Draw the state diagram and design a 3 bit up/down binary counter comprises a clocked sequential circuit having a level control input x and a clock input. It is required that when x = 0 the counter counts up and when x = 1 the counter counts down. (10)

b) Reduce the given state table using implication chart and obtain the equivalent states (10)

Present state	Next State		Output	
	X=0	X=1	X=0	X=1
A	A	B	0	0
B	D	C	0	1
C	F	E	0	0
D	D	F	0	0
E	B	G	0	0
F	G	C	0	1
G	A	F	0	0

****